REMARKS

The rejections presented in the Office Action dated June 29, 2005 have been considered. Claims 4 and 5 are amended to clarify the invention, and claim 27 is canceled for purposes of expediting prosecution. Claims 1, 3-9, 16-18, 20-21, and 23-26 are pending in the application. Reconsideration and allowance of the application are respectfully requested.

The Office Action does not establish that claims 1, 3-9, 16-18, 20, 21, and 23-26 are unpatentable under 35 USC §103(a) over "Cooper" ("Enhanced Code Compression for Embedded RISC Processors" by Cooper et al.) in view of "Haraguchi" (U.S. Patent No. 6,074,433 to Haraguchi et al.) and further in view of "Powell" (U.S. Patent No. 5,606,698 to Powell). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Cooper with teachings of Haraguchi and Powell, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action fails to show that the Cooper-Haraguchi-Powell combination suggests all the limitations of the claims. For example, claim 1 includes limitations of converting in the program code, each data reference in each keyword statement to a data array reference, and these limitations are not shown to be suggested by the combination.

Haraguchi teaches that multiple program loops with different array references may be merged into a single program loop. This is not suggestive of converting a keyword statement to a data array reference. Furthermore, the cited teaching of Haraguchi shows that the array references stay the same and are combined into a single loop; there is no apparent converting of a keyword statement to a data array reference. Since Haraguchi's data array references stay the same, there is no converting of a keyword statement to a data array reference. Similar limitations are found in independent claims 16, 21, 26. Thus, the Office Action fails to show that all the limitations of claims 1, 16, 21, and 26 are suggested by the Cooper-Haraguchi-Powell combination.

The alleged motivation for modifying Cooper with teachings of Haraguchi is improper and does not support a *prima facie* case of obviousness. The alleged motivation is that "it would have been obvious ... to supplement the method of Cooper to convert, in the program code, each data reference in each keyword statement to a data array reference, such as taught by Haraguchi, so as to optimize execution performance." No evidence is presented to demonstrate how supplementing teachings of Cooper with teachings from Haraguchi would further optimize the execution performance.

Cooper apparently teaches one approach for optimizing code (procedural abstraction and cross jumping), and Haraguchi teaches another approach (merging of loops involving arrays, Abstract). Cooper and Haraguchi teach separate approaches that may be individually applied. There is no apparent evidence to merit any particular modification to Cooper with teachings of Haraguchi in order to achieve the claimed invention. The references appear to suggest separate application of each approach to optimize code, and there is no apparent suggestion or evidence presented that demonstrates the manner in which Cooper could be modified with teachings of Haraguchi. Thus, the alleged motivation is unsupported by evidence and improper.

There is no evidence presented, nor is it apparent how a combination could be made with a reasonable likelihood of success by modifying Cooper with teachings of Haraguchi, even though the approaches of Cooper and Haraguchi may be individually applied to optimize code.

In regards to other limitations of claim 1, for example, those skilled in the art will also recognize that a procedure call would not "operate as a program loop when consecutive repeated patterns are replaced and executed in succession...", contrary to the assertion in the Office Action. Thus, the alleged motivation for modifying Cooper with teachings of Powell is improper and does not support a *prima facie* case of obviousness.

Claim 3 depends from claim 1 and includes further limitations related to converting each data reference to a data array reference. Thus, the limitations of claim 3 are not shown to be suggested by the Cooper-Haraguchi-Powell combination.

Claims 4, 5, 6, 7, 8, and 9 depend from claim 1 and are not shown to be unpatentable over the Cooper-Haraguchi-Powell combination for at least the reasons set forth above.

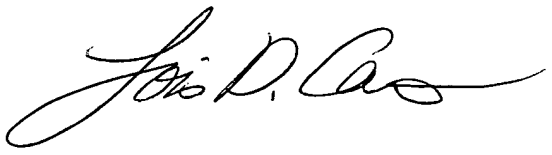
The rejection of claims 1, 3-9, 16-18, 20, 21, and 23-26 over the Cooper-Haraguchi-Powell combination should be withdrawn, because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

Claim 27 is now canceled, and the rejection of claim 27 as being unpatentable under 35 USC §103(a) over "Cooper" ("Enhanced Code Compression for Embedded RISC Processors" by Cooper et al.) in view of "Powell" (U.S. Patent No. 5,606,698 to Powell) is now moot.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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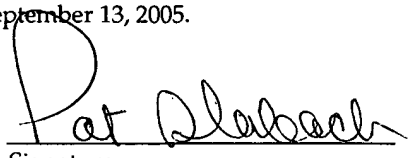
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